**WHAT IS CLAIMED IS**:

1. A circuit for signal transmission, said circuit comprising:

a current source;

a current sink having a current control terminal;

a current steering circuit having a pair of output nodes, said current steering circuit being arranged to receive current from the current source and to pass current to the current sink, and said current steering circuit being configured to provide a differential signal to a load connected across the output nodes; and

a control circuit including a voltage regulator, said voltage regulator being configured to produce a regulated voltage based on a comparison between a reference voltage and an offset voltage,

wherein the current control terminal of the current sink is arranged to receive the regulated voltage.

2. The circuit for signal transmission according to claim 1, wherein the current steering circuit includes two switches, each switch having an input node and one of the pair of output nodes and being configured to provide current to the respective output node or to receive current from the output node according to a potential at the input node.

3. The circuit for signal transmission according to claim 2, wherein each switch of the current steering circuit includes a first transistor and a second transistor, and

wherein the first transistor of each switch is configured and arranged to conduct current in response to a high potential at the respective input node and to be substantially nonconductive in response to a low potential at the respective input node, and

wherein the second transistor of each switch is configured and arranged to conduct current in response to a low potential at the respective input node and to be substantially nonconductive in response to a high potential at the respective input node.

4. The circuit for signal transmission according to claim 2, wherein each switch of the current steering circuit includes a first transistor and a second transistor, and

wherein each first transistor is a PMOS transistor and each second transistor is an NMOS transistor.

5. The circuit for signal transmission according to claim 4, wherein each of the first transistors is arranged to receive current from the current source, and wherein each of the second transistors is arranged to pass current to the current sink.

6. The circuit for signal transmission according to claim 1, the control circuit further comprising a transistor coupled to a current control terminal of the current source in a current mirror configuration.

7. The circuit for signal transmission according to claim 1, wherein the voltage regulator is an operational amplifier.

8. The circuit for signal transmission according to claim 1, the control circuit further comprising a pair of resistances in series, wherein the voltage regulator is arranged to obtain the offset voltage from the junction between the pair of resistances.

9. The circuit for signal transmission according to claim 1, wherein each exterior node of the pair of resistances is conductively coupled to a respective one of the output nodes of the current steering circuit.

10. The circuit for signal transmission according to claim 1, the control circuit further comprising a replicated current sink having a current control terminal conductively coupled to the current control terminal of the current sink, and a replicated current source.

11. The circuit for signal transmission according to claim 10, the control circuit further comprising a transistor coupled to a current control terminal of the current source in a current mirror configuration.

12. The circuit for signal transmission according to claim 10, wherein the voltage regulator is an operational amplifier.

13. The circuit for signal transmission according to claim 10, wherein the replicated current source has a channel width that is smaller than a channel width of the current source by a first proportion, and

wherein the replicated current sink has a channel width that is smaller than a channel width of the current sink by the first proportion.

14. The circuit for signal transmission according to claim 10, wherein said circuit includes at least one dummy transistor,

wherein said at least one dummy transistor is located at a position taken from the group consisting of beside the current source, beside the current sink, beside the replicated current source, beside the replicated current sink, between the current source and the replicated current source, and between the current sink and the replicated current sink.

15. The circuit for signal transmission according to claim 10, the control circuit further comprising a first replicated current-switching transistor and a second replicated current-switching transistor,

wherein the first replicated current-switching transistor is arranged to receive current from the replicated current source and the second replicated current-switching transistor is arranged to pass current to the replicated current sink.

16. The circuit for signal transmission according to claim 15, wherein the first replicated current-switching transistor is a PMOS transistor, and

wherein the second first replicated current-switching transistor is a NMOS transistor.

17. The circuit for signal transmission according to claim 15, the control circuit further comprising a pair of resistances in series,

wherein the first replicated current-switching transistor is conductively coupled to one exterior node of the pair of resistances, and

wherein the second replicated current-switching transistor is conductively coupled to the other exterior node of the pair of resistances.

18. The circuit for signal transmission according to claim 17, wherein the voltage regulator is arranged to obtain the offset voltage from the junction between the pair of resistances.

19. A control signal generator comprising:

a first control cell including

a first inverter arranged to invert a data signal, and

a first analog switch including an input terminal, an output terminal, a first control terminal, and a second control terminal; and

a second control cell including

a second inverter arranged to invert a signal complementary to the data signal, and

a second analog switch including an input terminal, an output terminal, a first control terminal, and a second control terminal;

wherein the first analog switch is arranged to receive the inverted data signal at the input terminal, and wherein the second analog switch is arranged to receive the inverted complementary data signal at the input terminal, and

wherein the first analog switch is arranged to receive a clock signal at the first control terminal and a signal complementary to the clock signal at the second control terminal, and wherein the second analog switch is arranged to receive a clock signal at the first control terminal and a signal complementary to the clock signal at the second control terminal, and

wherein the first analog switch is configured to have a closed state when the first control terminal is at a high potential and the second control terminal is at a low potential and to have an open state when the first control terminal is at a low potential and the second control terminal is at a high potential, and

wherein the second analog switch is configured to have a closed state when the first control terminal is at a high potential and the second control terminal is at a low potential and to have an open state when the first control terminal is at a low potential and the second control terminal is at a high potential.

20. The control signal generator according to claim 19, further comprising a third inverter arranged to receive the data signal and produce the complementary data signal, and a fourth inverter arranged to receive the clock signal and produce the complementary clock signal.

21. The circuit for signal transmission according to claim 1, wherein said circuit is embodied within an integrated circuit.

22. A low voltage differential signaling driver including the circuit for signal transmission according to claim 1.

23. The circuit for signal transmission according to claim 1, further comprising a display panel arranged to receive the differential signal.